Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **D4**
2. **D5**
3. **D6**
4. **D7**
5. **E1**
6. **Q2**
7. **Q1**
8. **VSS**
9. **Q0**
10. **D0**
11. **D1**
12. **D2**
13. **D3**
14. **GS**
15. **E0**
16. **VDD**

**.062”**

**3 2 1 16**

**MASK**

**REF**

**7 8 9 10 11**

**4**

**5**

**6**

**15**

**14**

**13**

**12**

**.062”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential: VDD or FLOAT**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .062” X .062” DATE: 8/17/21**

**MFG: SPRAGUE/ALLEGRO THICKNESS .025” P/N: CD4532B**

**DG 10.1.2**

#### Rev B, 7/1